BYPASS-ABLE CARRY CHAIN IN A PROGRAMMABLE LOGIC DEVICE

BACKGROUND

1. Field of the Invention

[0001] The present application relates to programmable logic devices, and more particularly to a bypass-able carry chain in a programmable logic device.

2. Related Art

[0002] A programmable logic device ("PLD") is a digital, user-configurable integrated circuit used to implement a custom logic function. For the purposes of this description, the term PLD encompasses any digital logic circuit configured by the end-user, and includes a programmable logic array ("PLA"), a field programmable gate array ("FPGA"), and an erasable and complex PLD. The basic building block of a PLD is a logic element (LE) that is capable of performing logic functions on a number of input variables. A LE is typically equipped with circuitry to programmably implement the "sum of products" logic or look-up table logic, as well as one or more registers to implement sequential logic. Conventional PLDs combine together large numbers of such logic elements through an array of programmable interconnects to facilitate implementation of complex logic functions. PLDs have found particularly wide application as a result of their combined low up front cost and versatility to the user.

[0003] In a typical PLD architecture, an arithmetic mode of the LE is provided to implement faster arithmetic. In this mode, carry-chain logic is used between LEs to provide a fast rippling carry chain through a series of LEs, with each LE implementing a bit-slice of the arithmetic.

[0004] For example, with reference to FIG. 1, a typical PLD architecture 100 is depicted. PLD architecture 100 includes an array of logic elements (LEs) 102. Sets of LEs 102 are grouped together as logic array blocks (LABs) 104. A LAB 104 includes a carry chain 108, which connects the set of LEs in LAB 104. As depicted in FIG. 1, a carry-input signal (C_{in}) enters through the first LE 102 in LAB 104, propagates serially through each LE 102, then a carry-out signal (C_{out}) exits through the last LE 102. Because carry chain 108 propagates serially through each LE 102 in LAB 104, each LE 102 within LAB 104 is forced to be in arithmetic

mode, unless carry chain 108 is broken within LAB 104. Breaking a carry chain 108, however, can increase the delay for the logic and result in waste since the LEs 102 following the break in the carry chain 108 can not be used to perform other functions.

[0005] As also depicted in Fig. 1, PLD architecture 100 includes a number of input lines 106 into LAB 104. The number of input lines 106 for a LAB 104 is typically determined based on the typical usage rather than the maximum usage of LAB 104. Thus, a complex arithmetic operation may require more inputs per LE 102 than the typical usage, which can result in insufficient number of input lines 106 to fully support the carry chain.

SUMMARY

[0006] In one exemplary embodiment, a carry chain in a logic array block includes a first path connecting a first series of logic elements in the logic array block, where the logic elements in the first series is a subset of the set of logic elements in the logic array block. The carry chain also includes a second path connecting a second series of logic elements in the logic array block, where one or more of the logic elements in the second series are not in the first series.

DESCRIPTION OF DRAWING FIGURES

[0007] The present application can be best understood by reference to the following description taken in conjunction with the accompanying drawing figures, in which like parts may be referred to by like numerals:

[0008] FIG. 1 is a block diagram of a conventional programmable logic device (PLD) architecture;

[0009] FIGs. 2 - 6 are block diagrams of exemplary logic array blocks (LABs) with carry chains;

[0010] FIGs. 7 - 11 are block diagrams of exemplary LABs with carry chains and redundancy circuits;

[0011] FIG. 12 is a block diagram of exemplary LABs with redundancy circuits and carry select circuits;

[0012] FIGs. 13 and 14 are block diagrams of exemplary LABs with redundancy circuits, carry select circuits, and carry chains;

[0013] FIGs. 15 - 17 are block diagrams of exemplary LABs with carry chains having fixed bypass portions;

[0014] FIG. 18 is a block diagram of exemplary LABs with redundancy circuits, carry select circuits, and carry chains having fixed bypass portions;

[0015] FIG. 19 is a block diagram of exemplary LABs with metal layer option regions; and

[0016] FIG. 20 is a block diagram of an exemplary data processing system.

DETAILED DESCRIPTION

[0017] The following description sets forth numerous specific configurations, parameters, and the like. It should be recognized, however, that such description is not intended as a limitation on the scope of the present invention, but is instead provided as a description of exemplary embodiments.

[0018] I. Bypass-able Carry Chain

[0019] With reference to FIG. 2, in one exemplary embodiment a LAB 104 includes a set of LEs 102 and a carry chain 108. Carry chain 108 includes a first path connecting a first series of LEs 102 in LAB 104, where the LEs 102 in the first series is a subset of the LEs 102 in LAB 104. Carry chain 108 also includes a second path connecting a second series of LEs 102 in LAB 104, where one or more of the LEs 102 in the second series are not in the first series. In the present exemplary embodiment, the LEs 102 in the first series are a subset of the LEs 102 in the second series.

[0020] As depicted in FIG. 2, in the present exemplary embodiment, the first path includes only the top four LEs 102 in LAB 104. In the present exemplary embodiment, the second path includes the top four and bottom four LEs 102 in LAB 104. It should be recognized that LAB 104 can include any number of LEs 102, and the first path can include any number of LEs 102,

which are a subset of the set of LEs 102 in LAB 104. Additionally, it should be recognized that any number of LABs 104 can be arranged in an array as part of an exemplary PLD architecture.

[0021] Additionally, in the present exemplary embodiment, carry chain 108 includes one or more logic components to select between the first path and the second path. More particularly, in the exemplary embodiment depicted in FIG. 2, carry chain 108 includes a multiplexer 202 connected to a random access memory (RAM) bit 204 to select between a first input and a second input. Thus, carry chain 108 can be operated in a first mode and a second mode. When carry chain 108 is operated in the first mode, the first input of multiplexer 202 is selected and the carry signal is propagated through the first series of LEs 102. When carry chain 108 is operated in the second mode, the second input of multiplexer 202 is selected and the carry signal is propagated through the second series of LEs 102.

[0022] Again, as depicted in FIG. 2, when carry chain 108 is operated in the first mode, the carry signal propagates through only the top four of the eight LEs 102 in LAB 104. When carry chain 108 is operated in the second mode, the carry signal propagates through all eight LEs 102 in LAB 104. Thus, carry chain 108 is a bypass-able carry chain in that the bottom four LEs 102 in LAB 104 can be bypassed or excluded from carry chain 108. As described in greater detail below, the bypass-able portion of carry chain 108 can be located at any location (e.g., middle, top, etc.) within LAB 104.

[0023] In some applications, such as when the number of input lines into LAB 104 is sufficient for the arithmetic operation to be performed, all of the LEs 102 in LAB 104 can be used as part of carry chain 108 to perform the arithmetic operation. However, in some applications, such as when the number of input lines in LAB 104 is insufficient for the arithmetic operation to be performed, a subset of the LEs 102 in LAB 104 can be used as part of carry chain 108 to perform the arithmetic operation. The LEs 102 that are bypassed from carry chain 108 can then be used for various functions other than the arithmetic function being performed by carry chain 108. For example, the LEs 102 that are bypassed can be used in a logic mode while the LEs 102 in carry chain 108 can be used in an arithmetic mode.

[0024] II. Location of Bypass-able Portion

[0025] In the exemplary embodiment depicted in Fig. 2, the bottom portion of LAB 104 is bypass-able, meaning that one or more LEs 102 located in the bottom portion of LAB 104 can be bypassed from carry chain 108. It should be recognized, however, that the bypass-able portion of carry chain 108 can be located at any location within LAB 104.

[0026] For example, in another exemplary embodiment depicted in FIG. 3, the bypass-able portion of carry chain 108 is located at the top of LAB 104. More particularly, carry chain 108 includes a multiplexer 302 connected to a RAM bit 304 to select between a first input and a second input. When carry chain 108 is operated in a first mode, the first input of multiplexer 302 is selected and a carry signal is propagated through a first series of LEs 102. When carry chain 108 is operated in a second mode, the second input of multiplexer 302 is selected and a carry signal is propagated through a second series of LEs 102, where one or more of the LEs 102 in the second series are not in the first series. In the present exemplary embodiment, the LEs 102 in the first series are a subset of the LEs 102 in the second series.

[0027] In still another exemplary embodiment depicted in Fig. 4, the bypass-able portion of carry chain 108 is selectable between a first location and a second location within LAB 104. More particularly, carry chain 108 includes a first multiplexer 302 connected to a first RAM bit 304 to select between a first input and a second input of first multiplexer 302. Carry chain 108 also includes a second multiplexer 202 connected to a second RAM bit 204 to select between a first input and a second input of second multiplexer 202. The first multiplexer 302 can be used to bypass a first series of LEs 102 located in the top portion of LAB 104. The second multiplexer 202 can be used to bypass a second series of LEs 102 located in the bottom portion of LAB 104.

[0028] III. Location of Logic Components

[0029] In the exemplary embodiments depicted and described thus far, the logic components used to bypass the LEs in a portion of the LAB have been located in the middle of the LAB. It should be recognized, however, that these logic components can be located at various locations in the LAB.

[0030] For example, in an exemplary embodiment depicted in FIG. 5, multiplexer 202 is located at the bottom of LAB 104. In this exemplary embodiment, the bypass-able portion of carry chain 108 is located at the bottom of LAB 104.

[0031] In another exemplary implementation depicted in FIG. 6, multiplexer 202 is located at the top of LAB 104. In this exemplary implementation, the bypass-able portion of carry chain 108 is located at the bottom of LAB 104. Additionally, in this exemplary implementation, multiplexer 202 in a subsequent LAB 104 in carry chain 108 controls the bypassing of LEs 102 in a preceding LAB 104 in carry chain 108.

[0032] For example, as depicted in FIG. 6, assume that carry chain 108 propagates from LAB 104 (N) to LAB 104 (N+1). Thus, multiplexer 202 in LAB 104 (N+1) controls the passing of LEs 102 in LAB 104 (N).

[0033] IV. Row Redundancy

[0034] With reference to Fig. 7, in one exemplary embodiment, LAB 104 includes carry chain 108 and a redundancy circuit 700. As described above, an exemplary PLD architecture can include an array of LEs 102 and LABs 104. In the present exemplary embodiment, redundancy circuit 700 can be used to skip a LAB 104 in a column of LABs 104.

[0035] More particularly, redundancy circuit 700 includes a multiplexer 702 connected to a redundancy signal 704 to switch between a first input and a second input. The first input is connected to the output of carry chain 108 from a preceding LAB 104 in a preceding row. The second input is connected to the first input of a multiplexer 702 from a redundancy circuit 700 in a preceding LAB 104 in a preceding row. The output of multiplexer 702 is connected to carry chain 108. Thus, carry chain 108 can receive, as an input, the output of carry chain 108 from a preceding LAB 104 in a preceding row, which continues the carry chain from the preceding LAB 104. Alternatively, carry chain 108 can receive, as an input, the input into the redundancy circuit 700 in the preceding LAB 104 in the preceding row, which results in the preceding LAB 104 in the preceding row being skipped.

[0036] For example, as depicted in FIG. 7, a first input of multiplexer 702 in LAB 104 (N) is connected to the output of carry chain 108 from preceding LAB 104 (N-1) in a preceding row. A

second input of multiplexer 702 in LAB 104 (N) is connected to input of multiplexer 702 in preceding LAB 104 (N-1). Thus, when the first input of multiplexer 702 in LAB 104 (N) is selected using redundancy signal 704, the output of carry chain 108 from preceding LAB 104 (N-1) is propagated to carry chain 108 in LAB 104 (N). However, when the second input of multiplexer 702 in LAB 104 (N) is selected using redundancy signal 704, the input of multiplexer 702 in the preceding LAB 104 (N-1) is received as an input to carry chain 108 in LAB 104 (N), which results in carry chain 108 in the preceding LAB 104 (N-1) being skipped.

[0037] In the present exemplary embodiment, redundancy signal 704 can be created from hardware that determines if a row of LABs 104 is defective and needs to be skipped. For example, laser-programmed fuses can be used to determine if a row of LABs 104 is defective during initialization of the device.

[0038] In the exemplary embodiment depicted in Fig. 7, the bypass-able portion of carry chain 108 is located in the bottom portion of LAB 104. As noted earlier, it should be recognized that the bypass-able portion of carry chain 108 can be located at various locations of LAB 104.

[0039] For example, in another exemplary embodiment depicted in Fig. 8, redundancy circuit 700 is connected to a carry chain 108 with a bypass-able portion located at the top portion of LAB 104. In the present exemplary embodiment, carry chain 108 includes a 3:1 multiplexer 802 connected to a RAM bit 804 and a redundancy signal 806 to select between a first input, a second input, and a third input. When the preceding LAB 104 (N-1) is not skipped and the bypass-able portion located at the top portion of LAB 104 (N) is not bypassed, the first input of multiplexer 802 is selected and a carry signal is propagated from carry chain 108 from the preceding LAB 104 (N-1) through a first set of LEs 102 in LAB 104 (N). When the preceding LAB 104 (N-1) is skipped and the bypass-able portion located at the top portion of LAB 104 (N) is not bypassed, the first input of multiplexer 802 is also selected. When the preceding LAB 104 (N-1) is not skipped and the bypass-able portion located at the top portion of LAB 104 (N) is bypassed, the second input of multiplexer 802 is selected and a carry signal is propagated from carry chain 108 from the preceding LAB 104 (N-1) through a second set of LEs 102 in LAB 104 (N), where the second set of LEs 102 is a subset of the LEs 102 in the first set of LEs 102. When the preceding LAB 104 (N-1) is skipped and the bypass-able portion located at the top portion of

LAB 104 (N) is bypassed, the third input of multiplexer 802 is selected and a carry signal is propagated from the first input of redundancy circuit 700 from a preceding LAB 104 (N-1) in a preceding row through the second set of LEs 102 in LAB 104 (N).

[0040] In still another exemplary embodiment depicted in Fig. 9, redundancy circuit 700 is connected to a carry chain 108 with a bypass-able portion that is selectable between a first location and a second location within LAB 104. More particularly, in addition to multiplexer 802, which is described above, carry chain 108 includes multiplexer 202, which can be used to bypass one or more LEs 102 located in the bottom portion of LAB 104.

[0041] In the exemplary embodiments depicted in FIGs. 7 - 9, the logic components used to bypass the LEs in a portion of the LAB have been located in the middle of the LAB. It should be recognized, however, that these logic components can be located at various locations in the LAB.

[0042] For example, in an exemplary embodiment depicted in FIG. 10, redundancy circuit 700 is connected to carry chain 108 with a 3:1 multiplexer 1002 located at the bottom of LAB 104. In this exemplary embodiment, the bypass-able portion of carry chain 108 is located at the bottom of LAB 104. Multiplexer 1002 is also connected to select signal 704 of redundancy circuit 700 and a RAM bit 1004 to select between a first input, a second input, and a third input.

[0043] In the present exemplary embodiment, when the current LAB 104 (N) is skipped, the first input of multiplexer 1002 is selected and a carry signal is propagated from carry signal 108 from the preceding LAB 104 (N-1) to the carry signal 108 of the next LAB 104 (N+1) to bypass the LEs 102 in LAB 104 (N). When the current LAB 104 (N) is not skipped and the bypass-able portion located at the bottom portion of LAB 104 (N) is not bypassed, the second input of multiplexer 1002 is selected and a carry signal is propagated from carry chain 108 from preceding LAB 104 (N-1) through a second series of LEs 102 in LAB 104 (N). When the current LAB 104 (N) is not skipped and the bypass-able portion located at the bottom portion of LAB 104 (N) is bypassed, the third input of multiplexer 1002 is selected and a carry signal is propagated from carry chain 108 from preceding LAB 104 (N-1) through a first series of LEs 102 in LAB 104 (N), where one or more of the LEs 102 in the second series are not in the first series. In the present exemplary embodiment, the LEs 102 in the first series is a subset of the second series.

[0044] In another exemplary embodiment depicted in FIG. 11, redundancy circuit 700 is connected to carry chain 108 with a 4:1 multiplexer 1102 located at the top of LAB 104. In this exemplary embodiment, the bypass-able portion of carry chain 108 is located at the bottom of LAB 104. Multiplexer 1102 is also connected to select signal 704 of redundancy circuit 700 and a RAM bit 1104 to select between a first input, a second input, a third input, and a fourth input. When the preceding LAB 104 (N-1) is skipped and the bypass-able portion located at the bottom of LAB 104 (N-2) is not bypassed, the first input of multiplexer 1102 is selected and a carry signal is propagated through a second series of LEs 102 in LAB 104 (N-2) to the carry signal 108 of LAB 104 (N) to bypass the LEs 102 in LAB 104 (N-1). When the preceding LAB 104 (N-1) is skipped and the bypass-able portion located at the bottom of LAB 104 (N-2) is bypassed, the second input of multiplexer 1102 is selected and a carry signal is propagated through a first series of LEs 102 in LAB 104 (N-2), where one or more of the LEs 102 in the second series are not in the first series. In the present exemplary embodiment, the LEs 102 in the first series is a subset of the second series. The carry signal is then propagated to the carry signal 108 of LAB 104 (N) to bypass the LEs 102 in LAB 104 (N-1). When the preceding LAB 104 (N-1) is not skipped and the bypass-able portion located at the bottom portion of LAB 104 (N-1) is not bypassed, the third input of multiplexer 1102 is selected and a carry signal is propagated through a second set of LEs 102 in LAB 104 (N-1). When the preceding LAB 104 (N-1) is not skipped and the bypass-able portion located at the bottom portion of LAB 104 (N-1) is bypassed, the fourth input of multiplexer 1102 is selected and a carry signal is propagated from a first set of LEs 102 in LAB 104 (N-1).

[0045] V. Carry Select

[0046] With reference to FIG. 12, in one exemplary embodiment, LAB 104 includes a carry select circuit 1200 and redundancy circuit 700. In the present exemplary embodiment, carry select circuit 1200 includes a multiplexers 1202 and 1204. As depicted in FIG. 12, multiplexer 1202 is connected to the output of multiplexer 702 of redundancy circuit 700. Thus, the output of multiplexer 702 functions as a carry select signal for multiplexer 1202. As also depicted in FIG. 12, multiplexer 1202 includes a first input and a second input. In the present embodiment, the first input includes a first pre-computed value for a first set of LEs 102. The second input includes a second pre-computed value for the first set of LEs 102. Thus, when the carry select

signal is a zero, the first input of multiplexer 1202 is selected. When the carry select signal is a one, the second input of multiplexer 1202 is selected.

[0047] Similarly, multiplexer 1204 is connected to the output of multiplexer 1202, which functions as a carry select signal for multiplexer 1204. As depicted in FIG. 12, multiplexer 1204 includes a first input and a second input. The first input includes a pre-computed value for a second set of LEs 102. The second input includes a second pre-computed value for the second set of LEs 102. Thus, when the carry select signal is a zero, the first input of multiplexer 1204 is selected. When the carry select signal is a one, the second input of multiplexer 1204 is selected.

[0048] With reference now to FIG. 13, in another exemplary embodiment, LAB 104 includes carry select circuit 1200, redundancy circuit 700, and carry chain 108. It should be recognized that carry select circuit 1200, redundancy circuit 700, and carry chain 108 can share components. For example, multiplexer 1302 is a component of both carry select circuit 1200 and carry chain 108.

[0049] As depicted in FIG. 13, multiplexer 1302 is connected to the output of multiplexer 702, which functions as a carry select signal for multiplexer 1302, and a RAM bit 1304. As also depicted in FIG. 13, multiplexer 1302 includes a first input, a second input, and a third input. The first input includes a pre-computed value for a first set of LEs 102. The second input includes a second pre-computed value for the first set of LEs 102. The third input is connected to the output of multiplexer 702. Thus, when the carry select signal is zero and the first set of LEs 102 is not bypassed, the first input of multiplexer 1302 is selected. When the carry select signal is one and the first set of LEs 102 is not bypassed, the second input of multiplexer 1302 is selected. When the first set of LEs 102 is bypassed, the third input of multiplexer 1302 is selected.

[0050] Similarly, multiplexer 1306 is connected to the output of multiplexer 1302, which functions as a carry select signal for multiplexer 1306, and a RAM bit 1308. As depicted in FIG. 13, multiplexer 1306 includes a first input, a second input, and a third input. The first input includes a pre-computed value for a second set of LEs 102. The second input includes a second pre-computed value for the second set of LEs 102. The third input is connected to the output of multiplexer 1302. Thus, when the carry select signal is zero and the second set of LEs 102 is not

bypassed, the first input of multiplexer 1306 is selected. When the carry select signal is one and the second set of LEs 102 is not bypassed, the second input of multiplexer 1306 is selected. When the second set of LEs 102 is bypassed, the third input of multiplexer 1306 is selected.

[0051] With reference to FIG. 14, in still another exemplary embodiment, LAB 104 includes carry select circuit 1200, redundancy circuit 700, and bypass-able carry chain 108. In contrast to the embodiment depicted in FIG. 13, in the present exemplary embodiment depicted in FIG. 14, the logic components include 2:1 multiplexers 1402 and 1404, NAND gates, and NOR gates. The NAND and NOR gates can be used to initialize carry chain 108. For a more detailed description of initializing a carry chain, see co-pending U.S. Patent Application Serial Number _________, entitled INITIALIZING A CARRY CHAIN IN A PROGRAMMABLE LOGIC DEVICE, filed on ______, the entire content of which is incorporated herein by reference.

[0052] VI. Fixed Bypass

[0053] With reference to FIG. 15, in an exemplary embodiment, LAB 104 includes redundancy circuit 700 and a carry chain with a fixed bypass. In the present exemplary embodiment, the carry chain in LAB 104 is split into dual carry chains 108a and 108b. As depicted in FIG. 15, carry chain 108a propagates a carry signal through a first series of LEs 102 in LAB 104. Carry chain 108b propagates a carry signal through a second series of LEs 102 in LAB 104. In the present exemplary embodiment, none of the LEs 102 in the second series are in the first series. As also depicted in FIG. 15, in the present exemplary embodiment, carry chains 108a and 108b can be implemented without using logic components, which reduces the delay in propagating the carry signal.

[0054] With reference to FIG. 16, in another exemplary embodiment, carry chains 108a and 108b are depicted in LAB 104 where the logic components (e.g., multiplexers) are located at the top of LAB 104. As depicted in FIG. 16, carry chain 108a propagates a carry signal through a first series of LEs 108 in LAB 104. Carry chain 108b propagates a carry signal through a second series of LEs 102 in LAB 104. The PLD architecture also includes a redundancy circuits 700.

[0055] With reference to FIG. 17, in still another exemplary embodiment, carry chains 108a and 108b are depicted in LAB 104 where multiplexers for LAB 104 are located at the bottom of

LAB 104. As depicted in FIG. 17, carry chain 108a propagates a carry signal through a first series of LEs 108 in LAB 104. Carry chain 108b propagates a carry signal through a second series of LEs 102 in LAB 104. The PLD architecture also includes a redundancy circuit 700.

[0056] With reference to FIG. 18, in still another embodiment, LAB 104 includes carry chains 108a and 108b, redundancy circuits 700, and carry select circuit 1200. As depicted in FIG. 18, carry chain 108a propagates a carry signal through a first series of LEs 102 in LAB 104. Carry chain 108b propagates a carry signal through a second series of LEs 102 in LAB 104. Carry select circuit 1200 includes a multiplexer 1802 connected to the output of multiplexer 702 of redundancy circuit 700, which functions as a carry select signal. As also depicted in FIG. 18, multiplexer 1802 includes a first input and a second input. The first input includes a first pre-computed value for the first set of LEs 102. The second input includes a second pre-computed value for the first set of LEs 102. Similarly, a multiplexer 1804 is connected to the output of multiplexer 702, which functions as a carry select signal. Multiplexer 1804 includes a first input and a second input. The first input includes a first pre-computed value for the second set of LEs 102. The second input includes a second pre-computed value for the second set of LEs 102.

[0057] VII. Metal Layer Options and Carry Chain Initialization

[0058] With reference to FIG. 19, in one exemplary embodiment, LAB 104 includes a carry chain 108 having metal layer option regions 1902. When the layout for LAB 104 is implemented, metal layer option regions 1902 can be formed in accordance with a first layout or a second layout. When metal layer option regions 1902 are formed in accordance with the first layout, the bypass-able region of carry chain 108 in LAB 104 is located in a first portion of LAB 104. When metal layer option regions 1902 are formed in accordance with the second layout, the bypass-able region of carry chain 108 in LAB 104 is located in a second portion of LAB 104.

[0059] For example, similar to the exemplary embodiment depicted in FIG. 8, in the exemplary embodiment depicted in FIG. 19, when metal layer option regions 1902 are formed with the solid lines, the bypass-able region of carry chain 108 in LAB 104 is located in the top portion of LAB 104. Similar to the exemplary embodiment depicted in FIG. 7, in the exemplary embodiment depicted in FIG. 19, when metal layer option regions 1902 are formed in accordance with the dashed lines, the bypass-able region of carry chain 108 in LAB 104 is

located in the bottom portion of LAB 104. Thus, a generic layout can be used for LAB 104, where only the layout within metal layer option regions 1902 are altered to determine the location of the bypass-able portion of carry chain 108.

[0060] As described above, an exemplary PLD architecture includes an array of LABs 104. In one exemplary embodiment, the location of the bypass-able portion of carry chain 108 is alternated between columns of LABs 104. For example, in a first column of LABs 104, the bypass-able portion of carry chain 108 can be located at the top of the LABs 104. In a second column adjacent to the first column, the bypass-able portion of carry chain 108 can be located at the bottom of the LABs 104. Alternating the location of the bypass-able portion of carry chain 108 between columns of LABs 104 can more evenly distribute the load on horizontal lines connecting the columns of LABs 104.

[0061] In the present exemplary embodiment, carry chain 108 can be initialized at a first location and a second location with LAB 104. In the exemplary embodiment depicted in FIG. 19, carry chain 108 can be initialized at a first location using RAM bits 1904 and at a second location using RAM bit 1906. For a more detailed description of initializing a carry chain, see co-pending U.S. Patent Application Serial Number _________, entitled INITIALIZING A CARRY CHAIN IN A PROGRAMMABLE LOGIC DEVICE, filed on ______, the entire content of which is incorporated herein by reference.

[0062] VIII. Data Processing System

[0063] With reference to FIG. 20, an exemplary PLD 2010 is depicted as a component of an exemplary data processing system 2000. PLD 2010 includes LABs 104 with LEs 102. (Only one LAB 104 and LE 102 are depicted to avoid overcomplicating the drawing.) Data processing system 2000 may include one or more of the following components: a processor 2040; memory 2050; input/out (I/O) circuitry 2020; and peripheral devices 2030. These components are coupled together by a system bus 2060 and are populated on a circuit board 2070, which is contained in an end-user system 2080.

[0064] It should be recognized that data processing system 2000 can be used in a wide variety of applications, such as computer networking, data networking, instrumentation, video

processing, digital signal processing, or any other application where the advantage of using programmable or reprogrammable logic is desirable. PLD 2010 can be used to perform a variety of different logic functions. For example, PLD 2010 can be configured as a processor or controller that works in cooperation with processor 2040 (or, alternatively, a PLD can act as the sole system processor). PLD 2010 may also be used as an arbiter for arbitrating access to a shared resource in system 2000. In yet another example, PLD 2010 can be configured as an interface between processor 2040 and one of the other components in system 2000.

[0065] Although exemplary embodiments have been described, various modifications can be made without departing from the spirit and/or scope of the present invention. Therefore, the present invention should not be construed as being limited to the specific forms shown in the drawings and described above.